REMARKS

This application has been carefully reviewed in light of the office action mailed December 4, 2002. New claims 31-38 have been added. Claims 1-18 and new claims 31-38 are pending in this application. Applicants respectfully request early and favorable acceptance of this application.

Rejections under 35 USC §102

Claims 1-18 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent 6,191,446 B1 issued to Mark I. Gardner et al. (hereinafter Gardner).

As amended Claim 1 recites, among other things, a semiconductor component comprising a drain region (e.g., 110) having a trench (e.g., 326). The drain region has a portion (e.g., 713) of a first conductivity type (e.g., n-type) and a first charge density. A region (e.g., 755) in the drain region has a second conductivity type (e.g., p-type) and a second charge density balancing the first charge density. A channel region (e.g., 120) of the second conductivity type is disposed in the drain region and adjacent to the trench.

The Gardner reference discloses in Fig.'s 3-12 and within columns 6-8 an integrated circuit having a substrate 40 formed with a trench 46, and having a first conductivity type (i.e., n-type). A channel is formed within the substrate adjacent to the trench. A source region 56, a lightly doped drain (LDD) region 60 and a drain region 66,

all having a second conductivity type (i.e., p-type) are also formed within the Gardner substrate.

The Gardner reference does not show or teach a drain region of a first conductivity type and having a first charge density, and a region of a second conductivity type in the drain region and having a second charge density balancing the first charge density as claimed. Neither of the Gardner drain regions 60 and 66 have regions of the opposite conductivity type formed within them. In particular, the reference does not teach a region formed in a drain region and having the opposite conductivity type.

Moreover, the reference is silent regarding the charge density of regions of the Gardner device. There is no suggestion in the reference of a region having a charge density balancing a charge density of a drain region, or charge density balancing the relative "size and volumes" of two conductive layers or regions to increase transistor power ratings as taught by the applicant in paragraphs 49-51. Indeed, the Gardner reference is directed towards the problem of controlling the channel length of a transistor by precisely etching a trench (column 8, lines 52-58) to provide the advantage of reducing short-channel and hot-carrier effects on transistor electrical performance (columns 1-2). The reference does not teach charge balancing as a method of alleviating these effects.

Therefore, claim 1, as amended, is not anticipated by the Gardner reference. Claims 2-18 depend from as amended claim 1, and are therefore allowable for at least the same reasons.

New claims 31-38 have been added.

New claim 31 recites among other things, a semiconductor component comprising a substrate (e.g., 105) having a first surface (e.g., 111) formed with first and second trenches (e.g., 326, 645). A drain region (e.g., 713) having a first conductivity type (e.g., n-type) is also formed adjacent to a bottom surface of the first trench. A charge balancing region (e.g., 755) having a second conductivity type (e.g., p-type) is formed adjacent to the drain region and along a sidewall of the second trench.

The Gardner reference does not disclose a substrate, a drain region having a first conductivity type disposed adjacent to a bottom of a first trench and a charge balancing region having a second conductivity type and formed adjacent to the drain region and adjacent to a second trench as claimed.

The bottom of the Gardner first trench 46 is formed adjacent to a source region 56, not a drain region. Moreover, the only region adjacent to the source or drain regions in the Gardner device is substrate 40, not a charge balancing region. Substrate 40 also extends to a region adjacent to second trench 38, so there cannot be a charge balancing region formed adjacent to second trench 40.

Therefore, new claim 31 is not anticipated by the Gardner reference. New claims 32-38 depend from new claim 31, and are allowable for at least the same reasons.

Applicants respectfully believe the rejection to have been overcome.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Conclusion

Applicants respectfully request entry of this amendment and early and favorable acceptance of this application.

Applicant has reviewed the other prior art made of record and believe that such art does not affect the patentability of the invention.

No fees are believed due by filing this Amendment. However, the Commissioner is authorized to charge any fees due or credit any overpayment to Deposit Account 501086.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney at the examiner's convenience.

Respectfully submitted,

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Version with Marking to Show Changes Made

IN THE CLAIMS

Please amend claim 1 as follows. Please add new claims 31-38 as follows.

1. (Amended) A semiconductor component comprising:

a [semiconductor layer]drain region having a trench with first and second sides, a portion of the [semiconductor layer]drain region having a first conductivity type and a first charge density;

a control electrode in the trench;

a channel region of the second conductivity type in the [semiconductor layer]drain region and adjacent to the trench; and

a first region in the [semiconductor layer]drain region, having a second conductivity type, and having a second charge density balancing the first charge density.

2. (Amended) The semiconductor component of claim 1, wherein:

the [semiconductor layer]drain region has a first surface and a second surface;

a first portion of the first region is at the first side of the trench and extends along a height of the [semiconductor layer]drain region from the first surface of the [semiconductor layer]drain region toward the second surface of the [semiconductor layer]drain region; and

a second portion of the first region is at the second side of the trench and extends along the height of the [semiconductor layer]drain region from the first surface of the [semiconductor layer]drain region toward the second surface of the [semiconductor layer]drain region.

6. (Amended) The semiconductor component of claim 5, wherein the first region is continuous from the first surface of the [semiconductor layer]drain region toward the second surface of the [semiconductor layer]drain region.

7. (Amended) The semiconductor component of claim 2, wherein:

the first region is contiguous with the first surface of the [semiconductor layer]drain region; and

the trench is in the second surface of the [semiconductor layer]drain region.

9. The semiconductor component of claim 1, further comprising an electrically insulative layer in the trench between the [semiconductor layer]drain region and the control electrode.

11. (Amended) The semiconductor component of claim 10, wherein:

the [semiconductor layer]drain region has a first surface and a second surface;

the trench is in the second surface of the [semiconductor layer]drain region; and

the semiconductor component further comprises a second region in the [semiconductor layer]drain region, at the second surface of the [semiconductor layer]drain region, having the first conductivity type, and contiguous with the trench.

12. (Amended) The semiconductor component of claim 1, wherein:

the [semiconductor layer]drain region has a first surface and a second surface;

the trench is in the second surface of the [semiconductor layer]drain region; and

the control electrode overlaps the second surface of the [semiconductor layer]drain region.

13. (Amended) The semiconductor component of claim 12, further comprising a second region in the [semiconductor layer]drain region, at the second surface of the [semiconductor layer]drain region, having the first conductivity type, and adjacent to and non-contiguous with the trench.

14. (Amended) The semiconductor component of claim 1, wherein the trench extends into the [semiconductor layer]drain region deeper than the channel region.

17. (Amended) The semiconductor component of claim 1, wherein the portion of the [semiconductor layer]drain region is located under the trench.

18. (Amended) The semiconductor component of claim 1, wherein:

the [semiconductor layer]drain region has a first surface and a second surface;

a first portion of the first region is at the first side of the trench and extends along a height of the [semiconductor layer]drain region from the first surface of the [semiconductor layer]drain region toward the second surface of the [semiconductor layer]drain region;

a second portion of the first region is at the second side of the trench and extends along the height of the [semiconductor layer]drain region from the first surface of the [semiconductor layer]drain region toward the second surface of the [semiconductor layer]drain region; and

the portion of the [semiconductor layer]drain region is located between the first and second portions of the first region.

31. (New) A semiconductor component comprising:

a substrate having a first surface formed with a first trench;

a drain region having a first conductivity type and formed over the substrate to define a second trench; and

a charge balancing region having a second conductivity type and formed adjacent to the drain region and along a sidewall of the first trench.

32. (New) The semiconductor component of claim 31 further comprising a dopant layer of the second conductivity type disposed within the first trench adjacent to the charge balancing region.

33. (New) The semiconductor component of claim 32, wherein the dopant layer is disposed between the sidewall of the first trench and the charge balancing region.

34. (New) The semiconductor component of claim 33, further comprising a channel region formed adjacent to a side of the second trench.

35. (New) The semiconductor component of claim 33, wherein the dopant layer includes in-situ boron-doped polysilicon or spin-on glass.

36. (New) The semiconductor component of claim 33, wherein the dopant layer includes doped boron nitride.

37. (New) The semiconductor component of claim 34 further comprising a control electrode formed within the second trench.

38. (New) The semiconductor component of claim 34 further comprising a source region formed at the first surface of the substrate adjacent to the channel region.